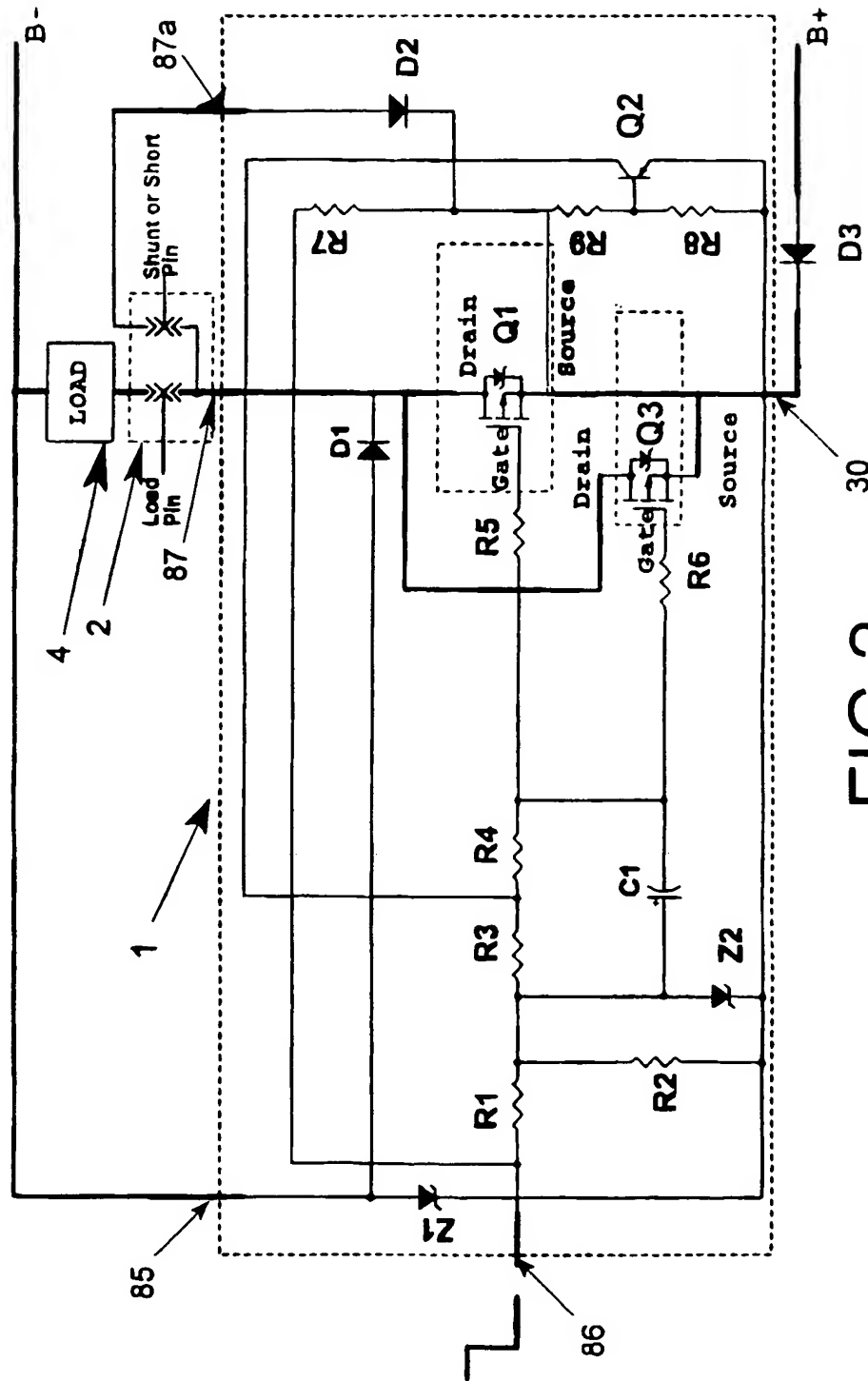


FIG 1



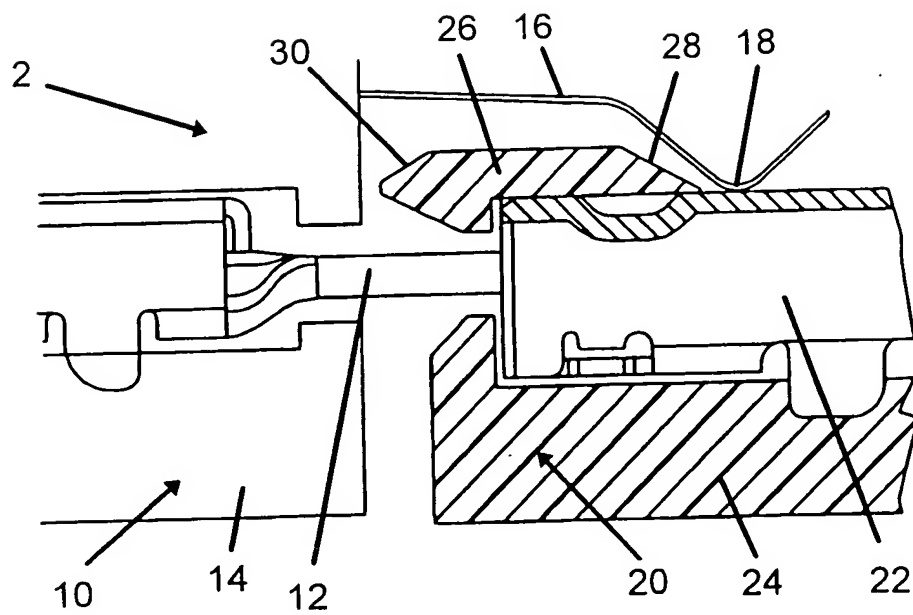


FIG 3

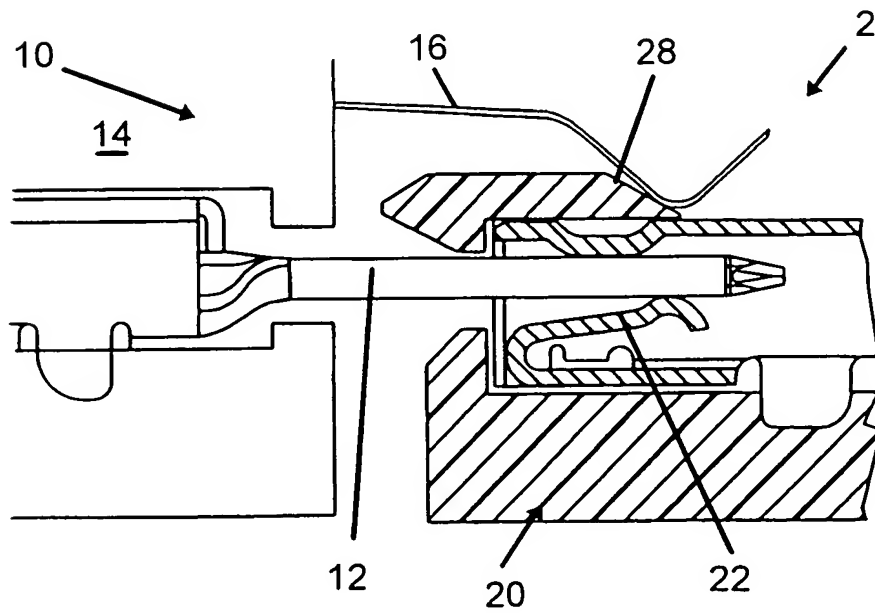


FIG 4

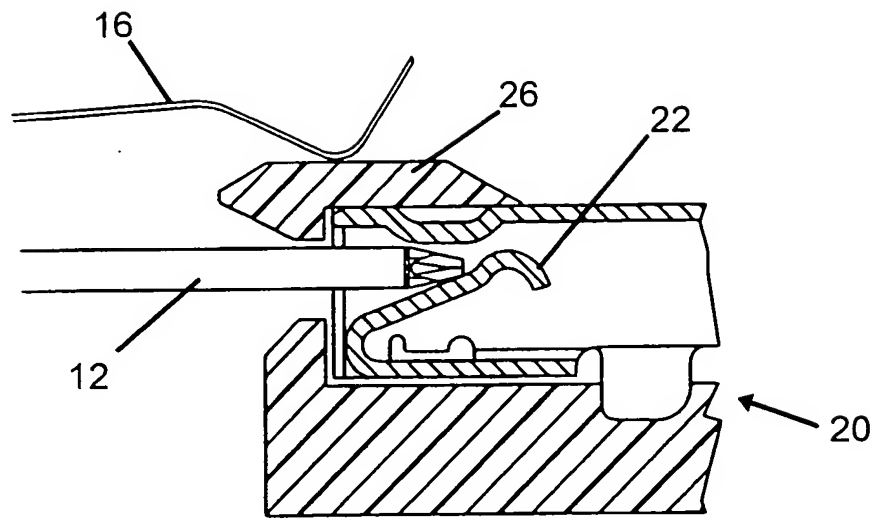


FIG 5

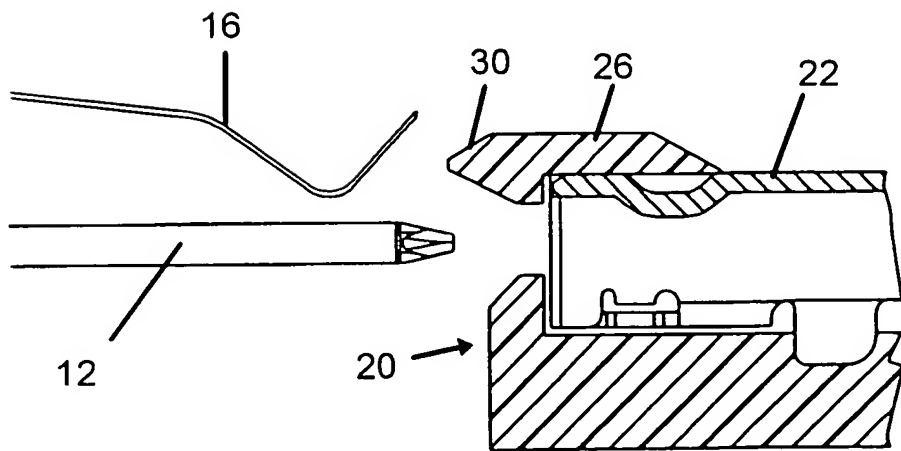
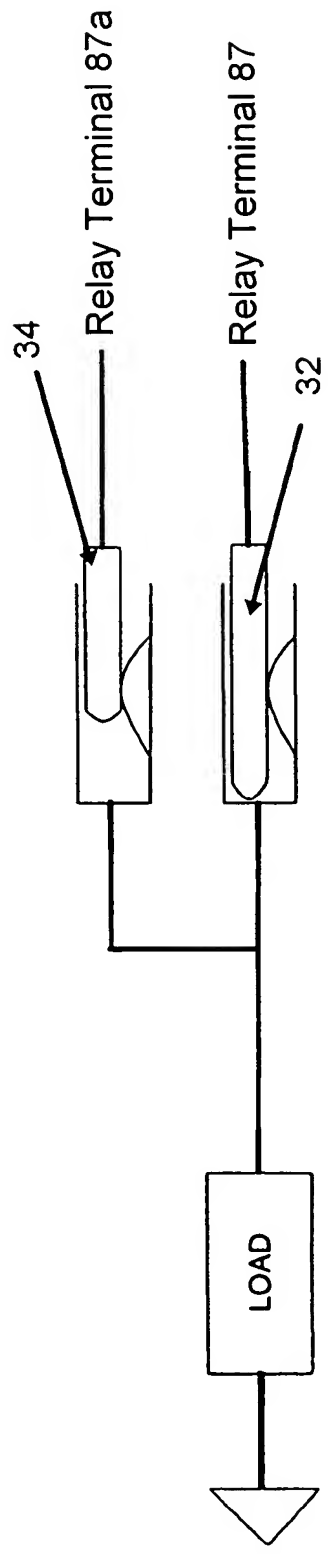


FIG 6

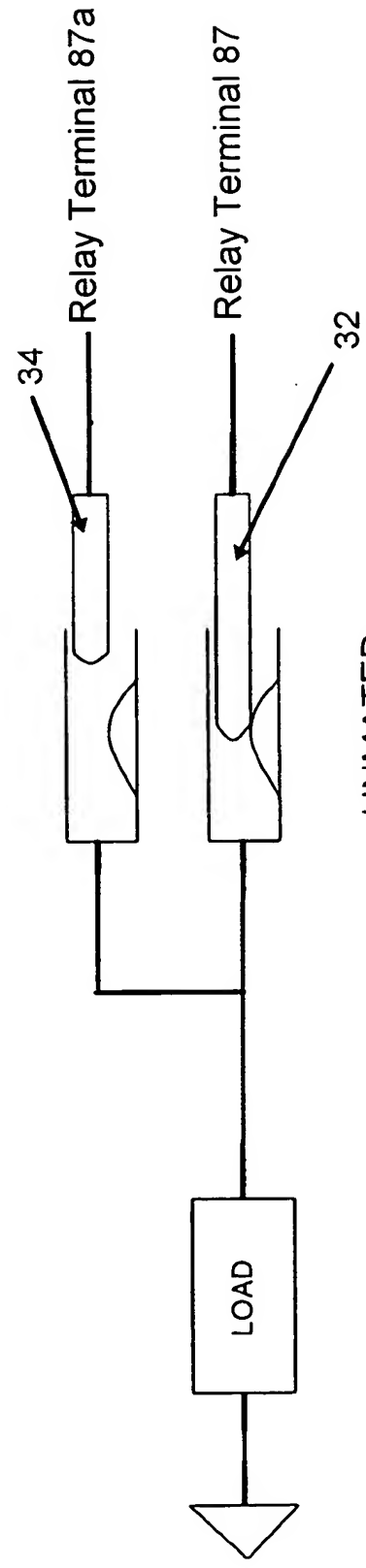
FIG. 7A is a schematic diagram of a relay assembly 2 in a mated state. The assembly includes a load 32, a relay terminal 87, and a relay terminal 87a. The relay terminal 87 is connected to the load 32, and the relay terminal 87a is connected to the relay terminal 87. The relay terminal 87a is shown in a position where it is engaged with the relay terminal 87, indicating a mated state.



MATED

FIG 7A

2



UNMATED

FIG 7B

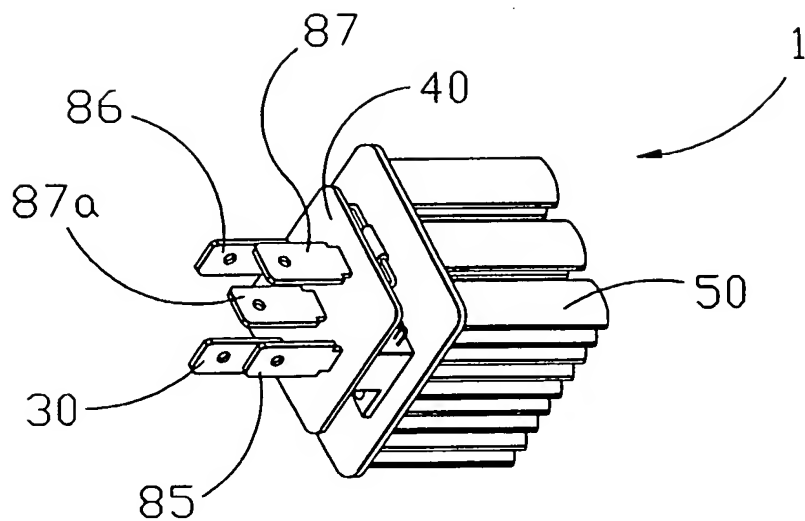


FIG 8

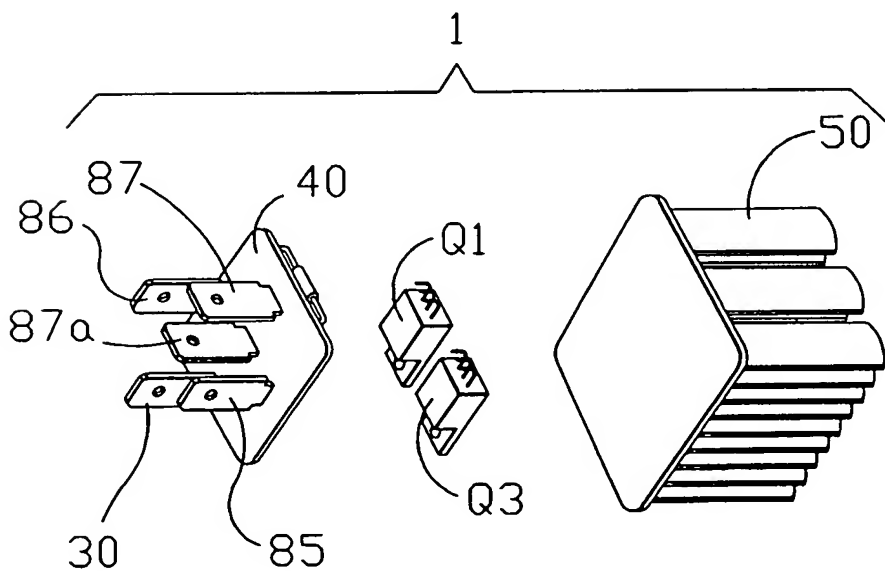


FIG 9

FIG. 10 is a schematic diagram of a power MOSFET driver circuit. The circuit includes a MOSFET Q1 with its gate connected to a gate driver circuit. The gate driver circuit consists of a network of resistors R1, R2, R3, R4, R5, R6, R8, and R9, and a capacitor C1. The MOSFET Q1 has its source connected to ground and its drain connected to a load (LOAD) and a diode D1. The load is connected to a positive supply voltage B+. The diode D1 is connected to the positive supply voltage B+ and the drain of Q1. The gate driver circuit is connected to the gate of Q1 and the positive supply voltage B+.

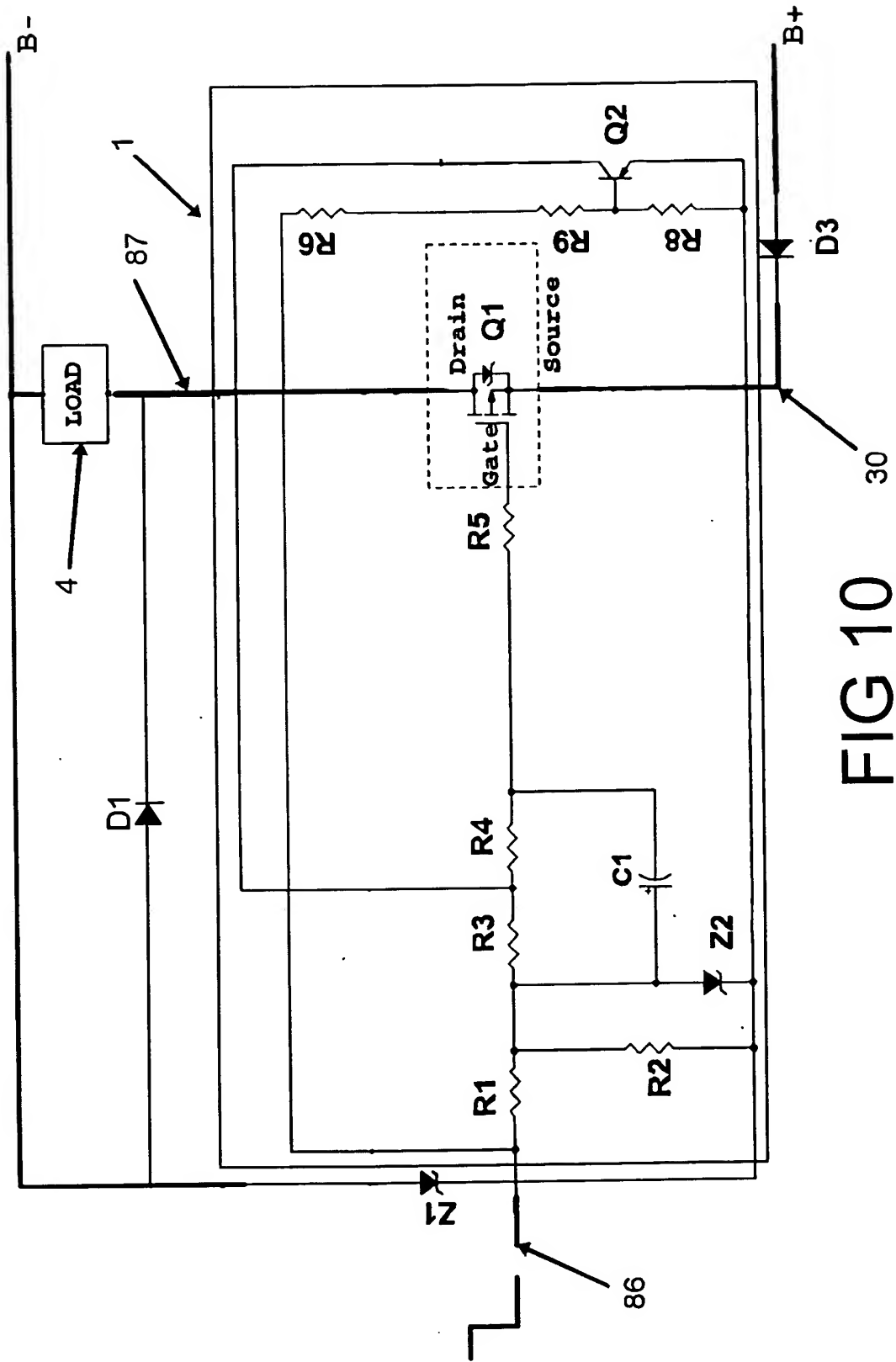


FIG 10

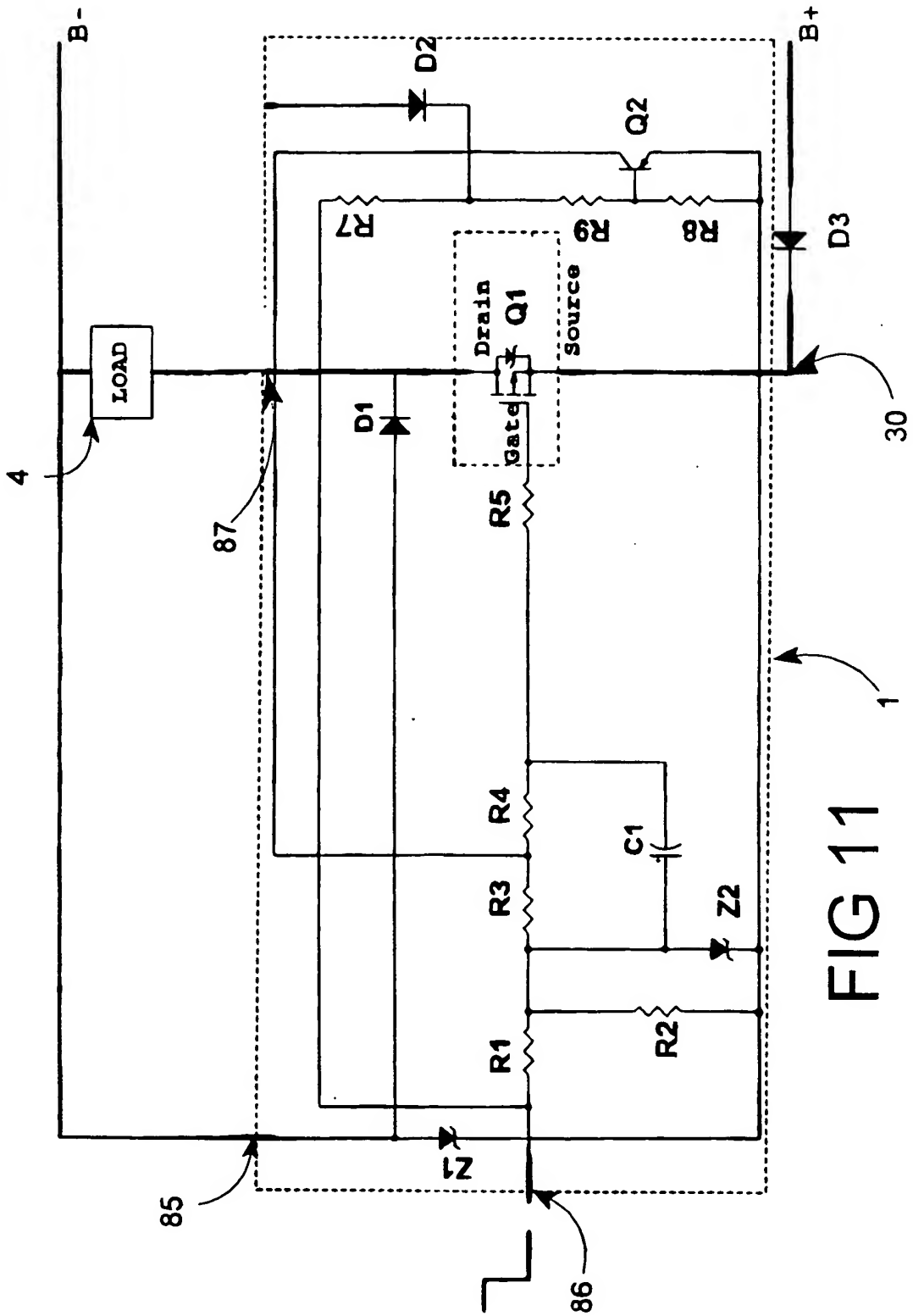


FIG 11

DIMENSIONS
INCH (MM.)

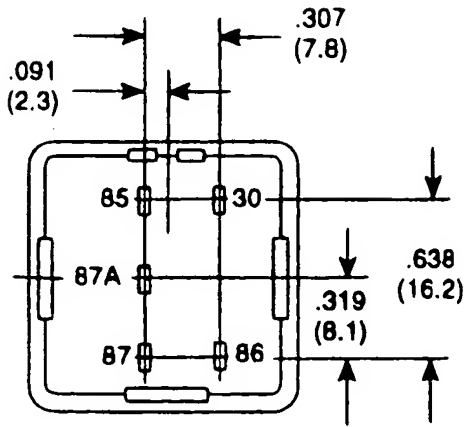


FIG 13
(PRIOR ART)

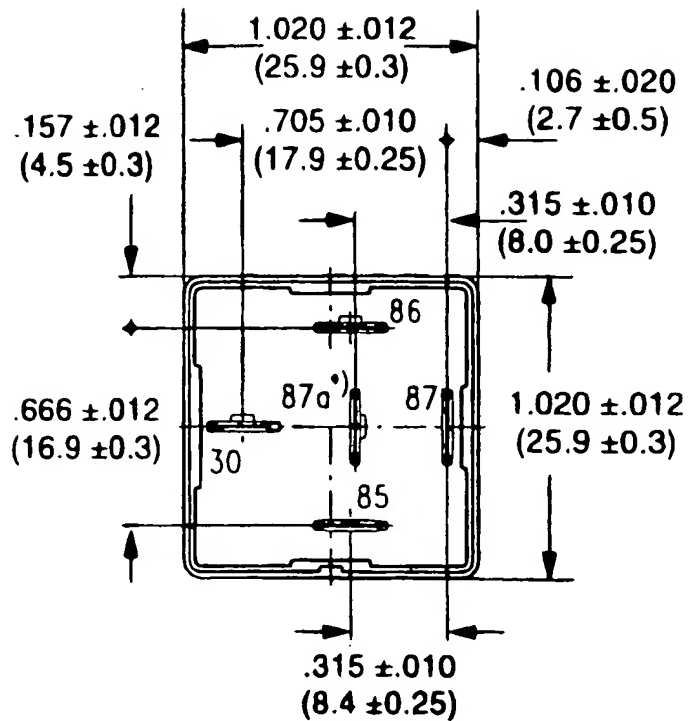


FIG 12
(PRIOR ART)

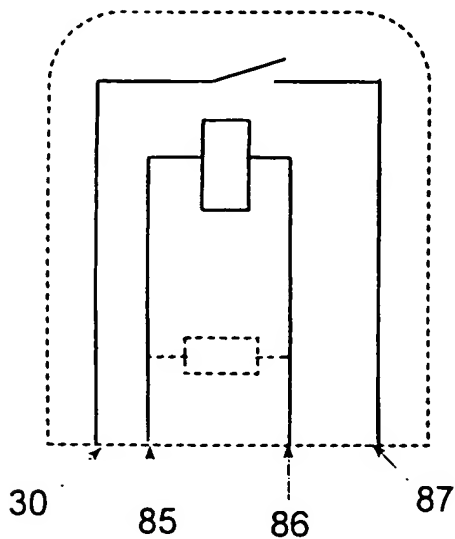


FIG 14
(PRIOR ART)

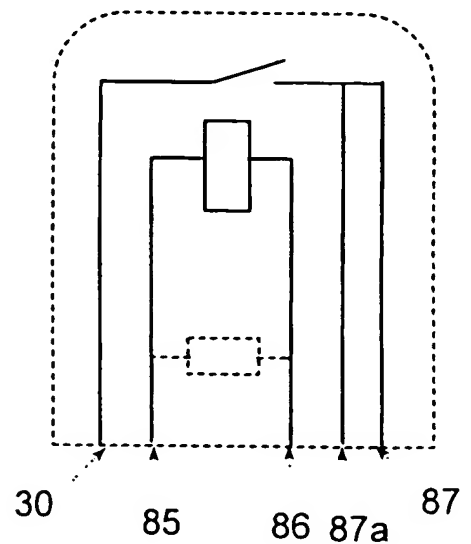


FIG 15
(PRIOR ART)